FIG. 1

(TABLE 1)

Timing Type	*Cell Delay [ps]*			
	Cell Rise	*Cell Fall*	*Transition Rise*	*Transition Fall*
Pre-layout	91 (-15.0%)	92 (-13.2.%)	46 (-13.2%)	45 (-11.8%)
Post-layout	107 (0.0%)	106 (0.0%)	53 (0.0%)	51 (0.0%)

5

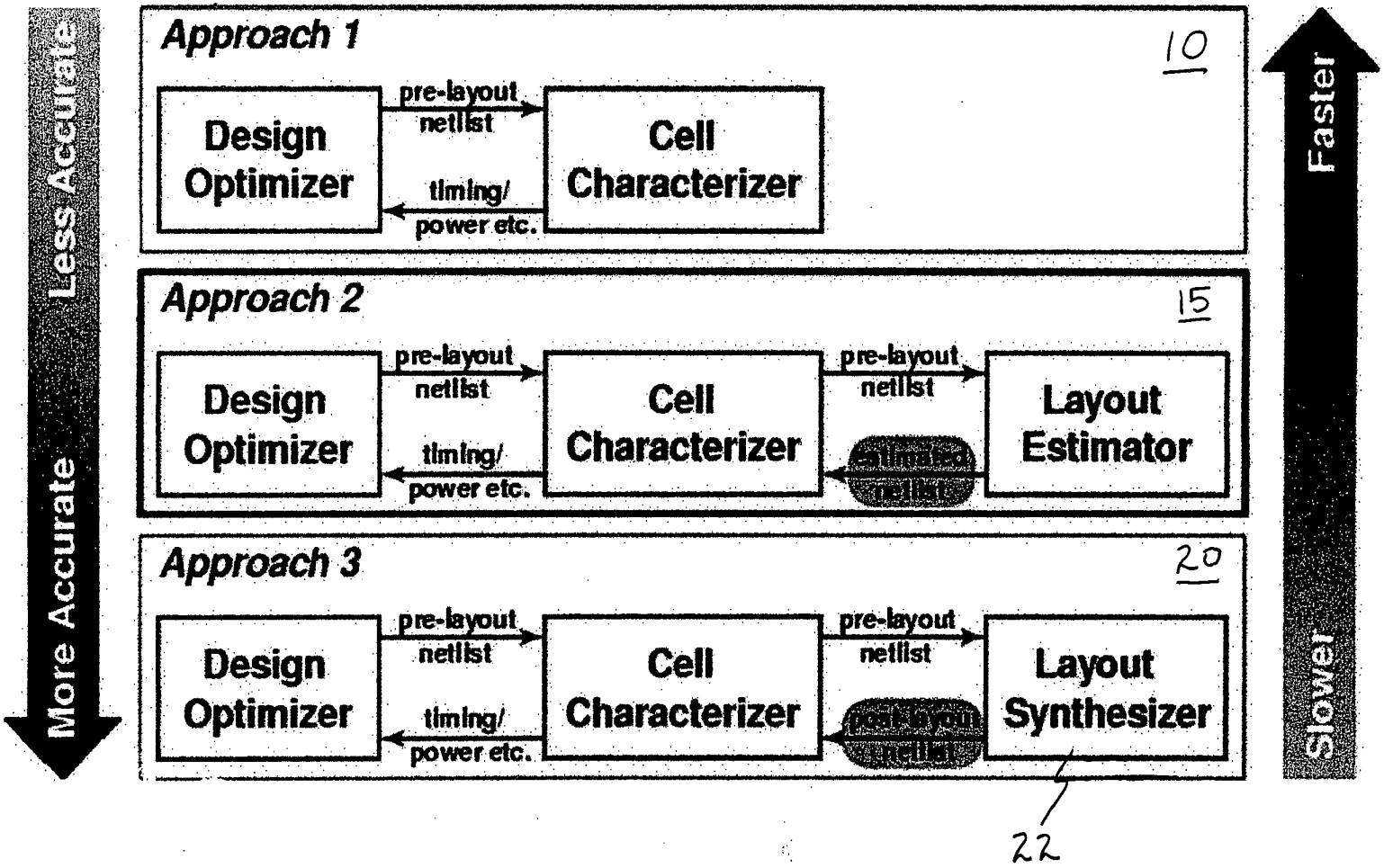

More Accurate
Less Accurate
Faster
Slower
Approach 1
10
Design Optimizer
pre-layout netlist
timing/ power etc.
Cell Characterizer
Approach 2
15
Design Optimizer
pre-layout netlist
timing/ power etc.
Cell Characterizer
pre-layout netlist
Layout Estimator
Approach 3
20
Design Optimizer
pre-layout netlist
timing/ power etc.
Cell Characterizer
pre-layout netlist
Layout Synthesizer
22

FIG. 2

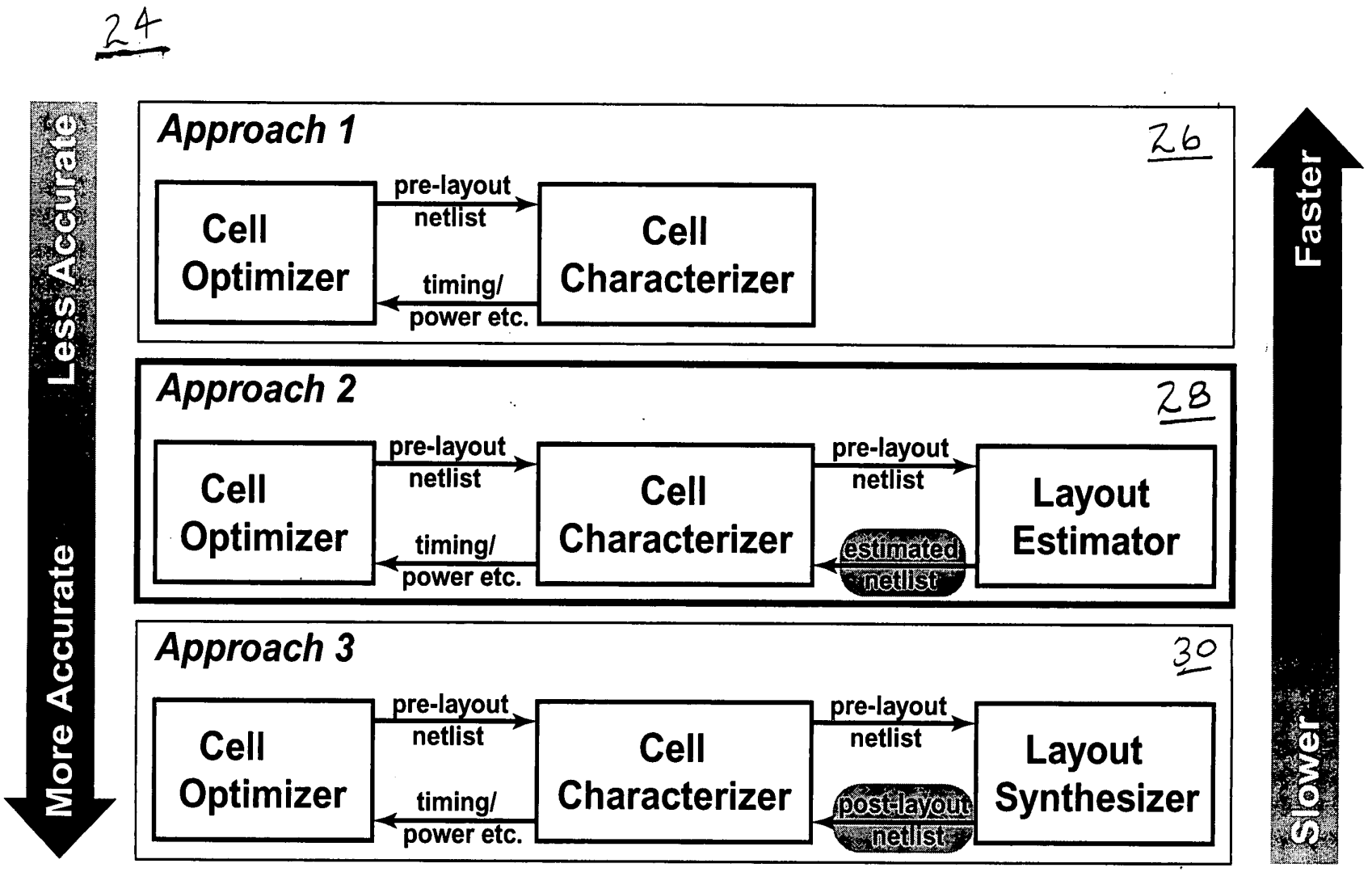

24
Less Accurate
More Accurate
Faster
Slower
Approach 1
26
Cell Optimizer
pre-layout netlist
timing/ power etc.
Cell Characterizer
Approach 2
28
Cell Optimizer
pre-layout netlist
timing/ power etc.
Cell Characterizer
pre-layout netlist
estimated netlist
Layout Estimator
Approach 3
30
Cell Optimizer
pre-layout netlist
timing/ power etc.
Cell Characterizer
pre-layout netlist
post-layout netlist
Layout Synthesizer

FIG. 3

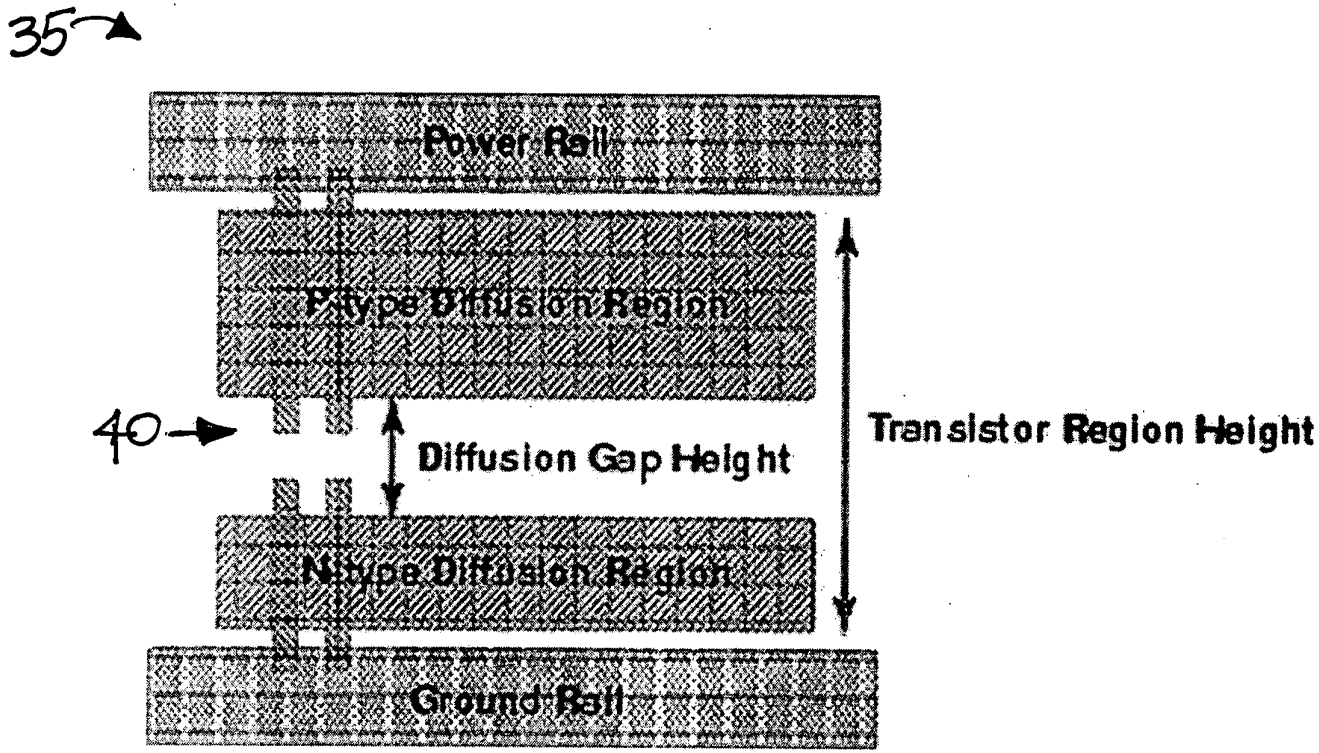
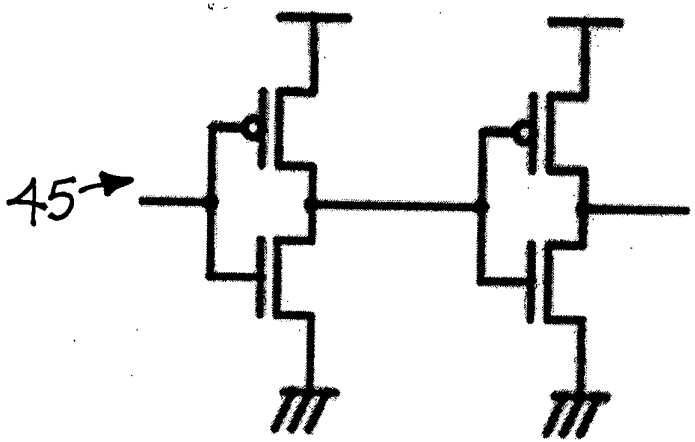

35
Power Rail
P type Diffusion Region
40
Diffusion Gap Height
Transistor Region Height
N type Diffusion Region
Ground Rail

FIG. 4

50

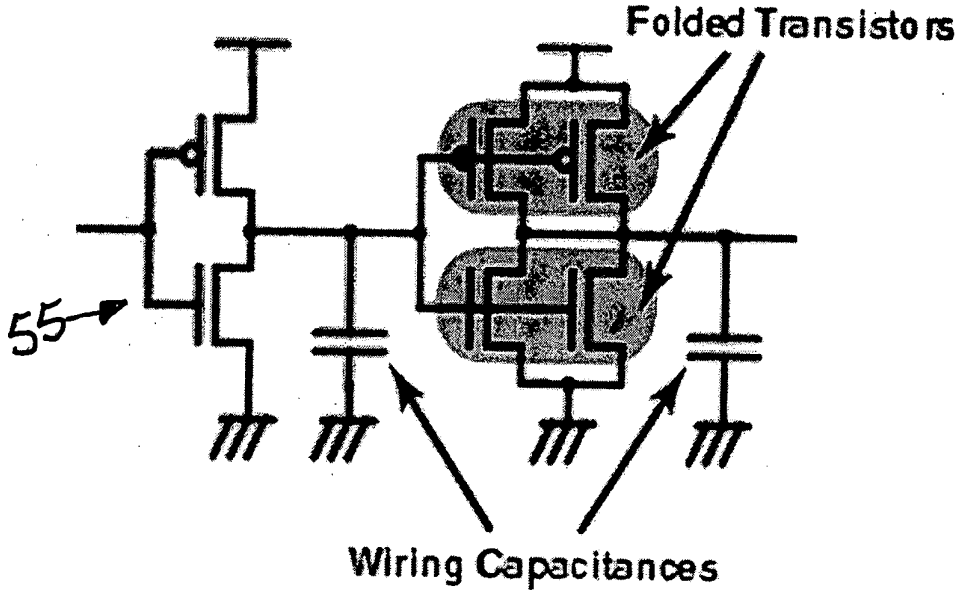
```
M1 n1 a vdd vdd p W=2.0u L=0.13u
                  :
```



5(a)

60

```
M1 n1 a vdd vdd p W=2.0u L=0.13u
+ AD=0.36e-12 AS=0.36e-12
+ PD=4.36e-6 PD=4.36e-6
                  :
C1 n1 vss 1.2f
                  :
```



5 (b)

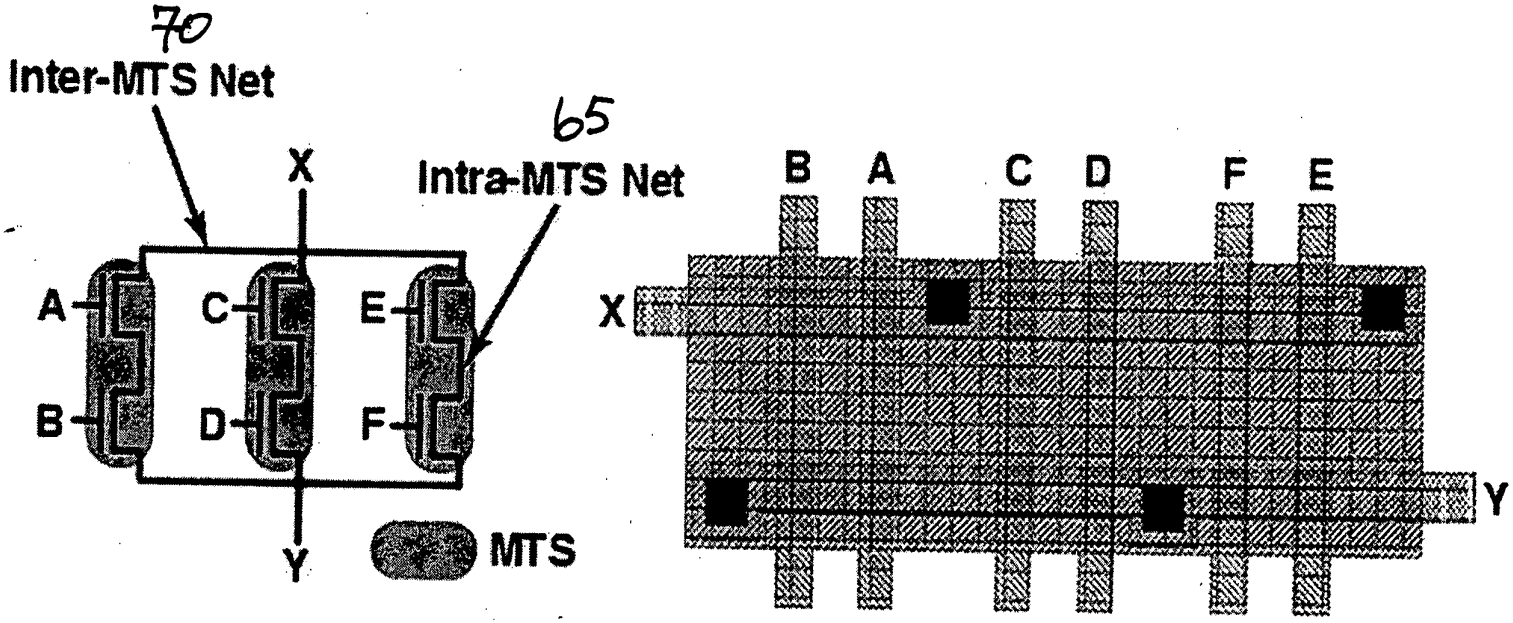
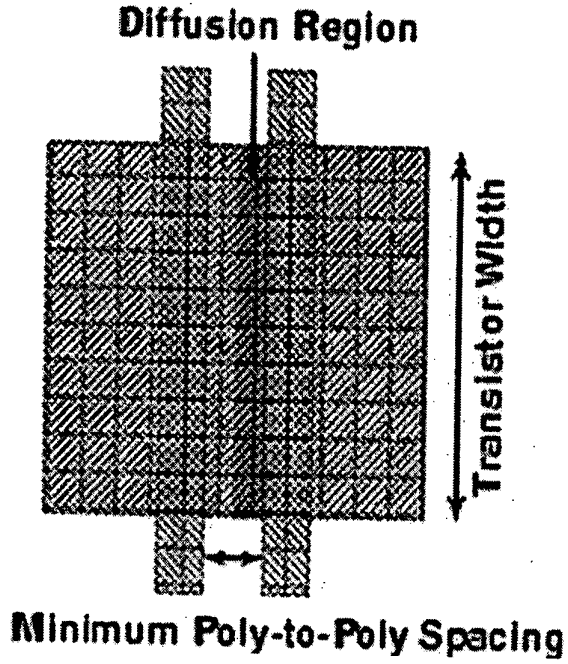
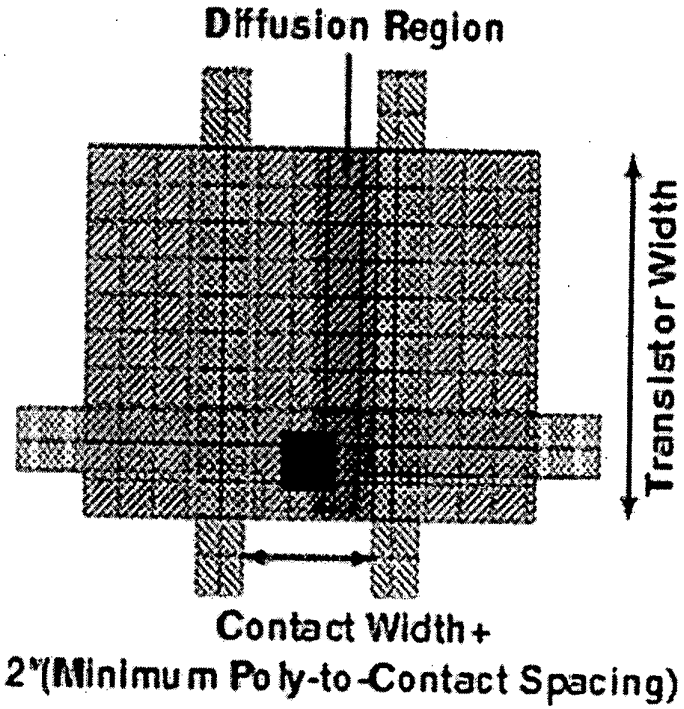


FIG. 6


Diffusion Region
Transistor Width
Minimum Poly-to-Poly Spacing

7(a)


Diffusion Region
Transistor Width
Contact Width +
2*(Minimum Poly-to-Contact Spacing)

7(b)

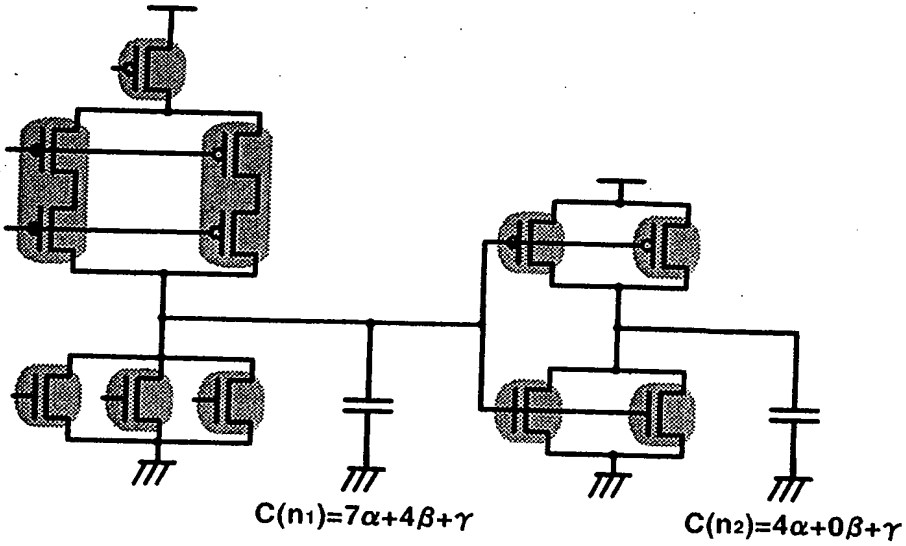
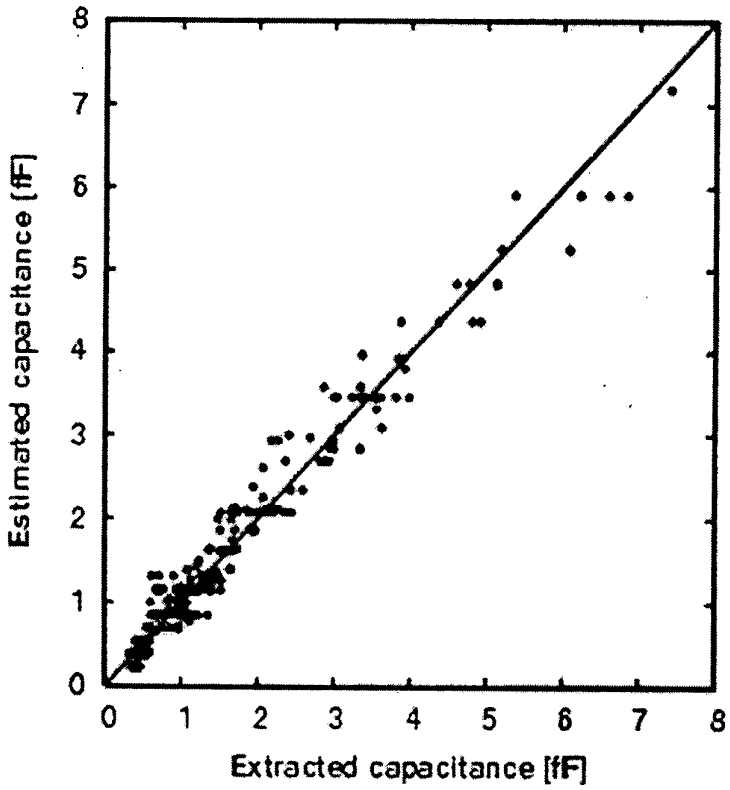


FIG. 8

9(a)


Estimated capacitance [fF]
Extracted capacitance [fF]
0
1
2
3
4
5
6
7
8

9(b)

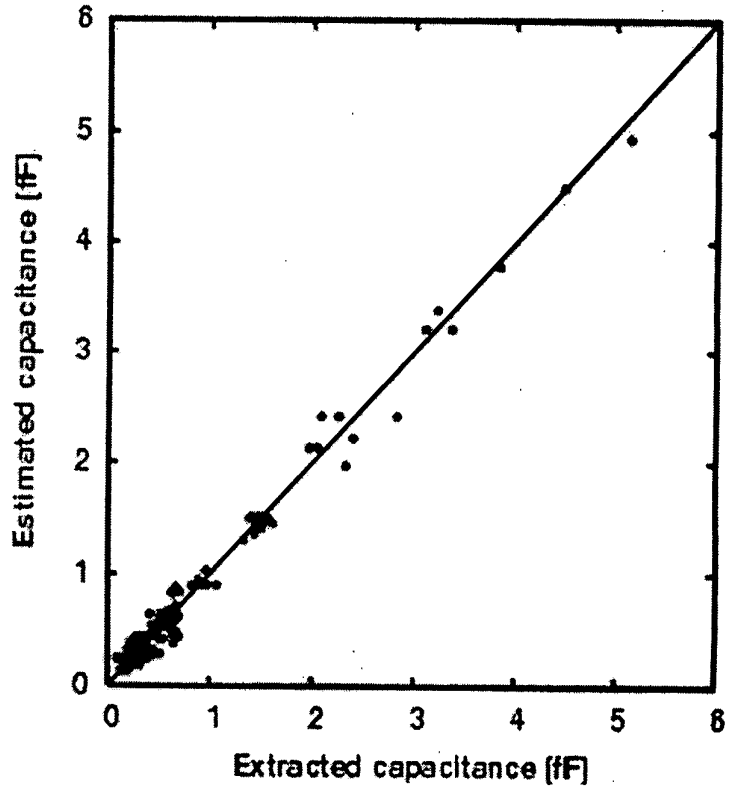

Estimated capacitance [fF]
Extracted capacitance [fF]
0
1
2
3
4
5
6

FIG 10

Table 2: Comparison of proposed estimation techniques.

Estimation Technique	*Cell Delay [ps]*			
	Cell Rise	*Cell Fall*	*Transition Rise*	*Transition Fall*
No Estimation	91 (-15.0%)	92 (-13.2%)	46 (-13.2%)	45 (-11.8%)
Statistical Estimator	100 (-6.5%)	101 (-4.7%)	51 (-3.8%)	49 (-3.9%)
Constructive Estimator	106 (-0.9%)	105 (-0.9%)	52 (-1.9%)	49 (-3.9%)
Post-layout	107 (0.0%)	106 (0.0%)	53 (0.0%)	51 (0.0%)

Table 3: Quality of proposed estimation techniques for two industrial standard cell libraries.

Feature Size [nm]	*#Cells*	*#Wires*	*No Estimation*		*Statistical Estimator*		*Constructive Estimator*	
			Avg. Abs. Diff. [%]	*Std. Dev. [%]*	*Avg. Abs. Diff. [%]*	*Std. Dev. [%]*	*Avg. Abs. Diff. [%]*	*Std. Dev. [%]*
130	57	276	8.85	4.08	3.60	2.76	1.55	1.79
90	53	221	8.81	4.80	4.10	3.35	1.52	1.40

FIG. 11